ABSTRACT

A technology for a semiconductor integrated circuitry allows each of the DRAM memory cells to be divided finely so as to be more highly integrated and operate faster. In a method of manufacturing such a semiconductor integrated circuit, at first, gate electrodes 7 are formed via a gate insulating film 6 on the main surface of a semiconductor substrate 1, and on side surfaces of each of the gate electrodes there is formed a first side wall spacer 14 composed of silicon nitride and a second side wall spacer 15 composed of silicon oxide. Then, in the selecting MISFET Qs in the DRAM memory cell area there are opened connecting holes 19 and 21 in a self-matching manner with respect to the first side wall spacers 14 and connecting portion is formed connecting a conductor 20 to a bit line BL. In addition, in the N channel MISFETs Qn1 and Qn2, and in the P channel MISFET Qp1 in areas other than the DRAM memory cell area, high density N-type semiconductor areas 16 and 16b are formed, as well as a high density P-type semiconductor area 17 is formed in a self-matching manner with respect to the second side wall spacers 15.